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Power Optimization for Ripple Carry Adder with Reduced Transistor Count

Manju Bala[1], Neeraj Gupta[2], Priti Singh[3]

[1] Student M. Tech. ECE, Amity University Haryana, India
[2,3]Assistant Professor, Amity University Haryana, India

Abstract: **The optimization of power dissipation has become one of the barriers for scaling of MOSFET to catch up ITRS roadmap. The life time of battery operated devices may be reduced due to the power. In CMOS nano regime technologies, power dissipation plays an important role. In most of the digital systems adder lies in the vital path that enhance the propagation delay of the system. This paper proposes a new three transistor based design with significant area and power savings for ripple carry adder. A comparative study and analysis of various power minimization techniques for ripple carry adder have been presented in this paper and the study shows that three transistor based design is more effective than other existing techniques. The result is validated by Eldo SPICE Simulator in Mentor Graphics at 0.35um CMOS process technology.**

Keywords: **TSMC0.35, Power Optimization, 3T XOR gate, Full Adder, Pseudo NMOS Logic, Ripple Carry Adder.**

1. INTRODUCTION

Day by day IC technology is getting advanced in terms of style, proportions and its performance exploration. A fast way with reduced leakage power and smaller planetary is implied to the latest electronic style. Addition is normally used mathematical process in silicon chip, DSP etc. It can be used as a basic block for synthesis of all arithmetic setups. The binary adder structure becomes an badly essential hardware unit. Even though several researches related with the binary adder structures are selected, the studies supported their comparative performance analysis area unit solely quite few in variety. During this project, we implement ripple carry adder using 3T technology which is very useful in reducing power consumption and simulate it using Eldo SPICE Simulator in Mentor Graphics at 0.35um CMOS process technology.

The 3 transistors based logic gates design is based on PMOS and NMOS Pass Transistor Logic (PTL). The 3T universal gates (NAND and NOR) design is based on CMOS inverter and PTL [4]. Output voltage deterioration occurs across the PMOS and NMOS because of threshold voltage drop while passing the logic 0 or logic 1 respectively in relation to the input. The voltage deterioration caused by threshold drop can be extensively minimized by increasing the W/L ratio of the pass transistor [4]. XOR gates form major building block of full adders. Improving the performance of the XOR gates can significantly enhance the performance of the adder. A survey of collected works discloses a wide range of different types of XOR gates that have been recognized over the years. The previous designs of XOR gates were designed by either eight transistors or six transistors that are usually used in most designs.

In this proposed work we are going to use XOR gate with 3T which can reduce its power consumption, increase its operating speed and reduce its size.

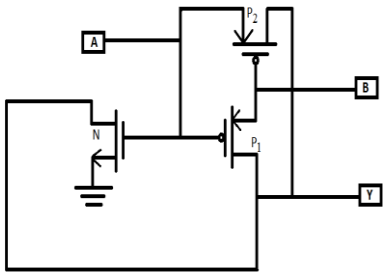


FIG.1: 3T BASED XOR GATE

WORKING:

- When A=B=0, P1 transistor becomes ON, N transistor becomes OFF and P2 transistor becomes ON. So at the output we get 0.
- When A=0, B=1, P1 transistor becomes ON, N transistor becomes ON and P2 transistor becomes OFF. So at the output we get 1.
- When A=1, B=0, P1 transistor becomes OFF, N transistor becomes ON and P2 transistor becomes ON. So at the output we get 1.
- When A=B=1, P1 transistor becomes OFF, N transistor becomes ON and P2 transistor becomes OFF. So at the output we get 0.

This is full working of 3T based XOR gate.

FULL ADDER:

Ever since its inception, the design of full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed.

The circuit produces a two-bit output, output carry and sum typically represented by the signals C_{out} and *Sum* [6], where

$$SUM = A \oplus B \oplus C_{IN} \quad \text{.....(1)}$$

$$C_{OUT} = (A*B) + [C_{IN}*(A+B)] \quad \text{.....(2)}$$

In this implementation, we use XOR gate with 3 transistors and in the place of two nand and or gate before carry out we are goimg to use 3 nand gates which are also fabricate by using three transistors.

As we know XOR gates are the basic building block of full adder and full adder is basic building block of ripple carry adder. So by reducing transistor count for full adder we can reduce transistor count for ripple carry adder, by which power dissipation will be optimized.

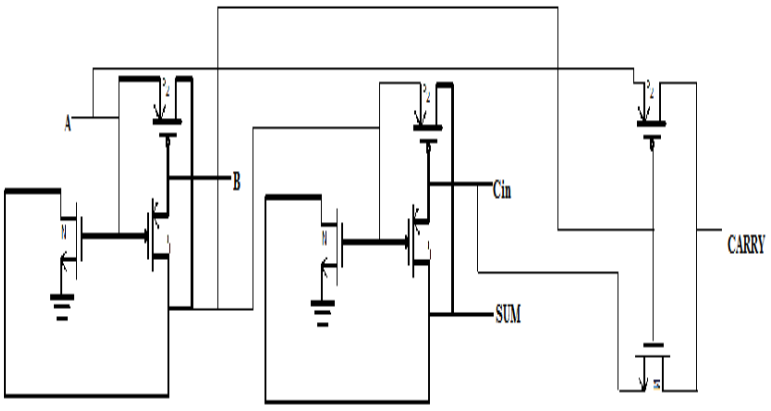


FIG.2: FULL ADDER USING 3T XOR GATE

So here we have built full adder with 15 transistors. For XOR=6 transistors, For NAND=9 transistors.

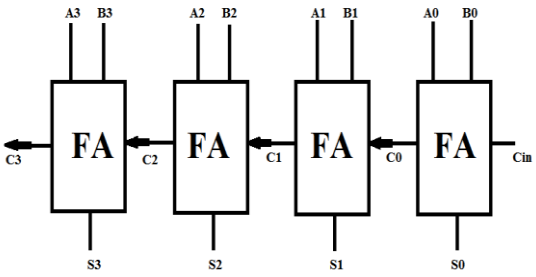
RIPPLE CARRY ADDER:

This popular adder design, ripple carry adder comprises of cascaded full adders. It is designed by cascading full adder blocks non-parallel with each other. The output carry of 1 stage works as input carry for second stage and so on[2].

The gate delay of ripple carry adder depends on total review or inspection of adder. As we know that each full adder needs 3 levels of logic.

In other words we can say full adder is basic building block of ripple carry adder[2]. In proposed work we have constructed full adder using 3T based logic gates.

The design of a ripple-carry adder is simple, which permits for fast design time; however, the ripple-carry adder is relatively slow[6], since each full adder need to wait for the carry bit to be calculated from the previous full adder as discussed above.



Ripple Carry Adder

2. SIMULATION AND PERFORMANCE ANALYSIS OF THE PROPOSED 3T XOR GATE

In this paper XOR gate shown is consisted of a CMOS inverter and an extra PMOS transistor. In which one input is given at gate voltage of additional PMOS transistor and source voltage of PMOS transistor of CMOS inverter and second input is gives at input of CMOS inverter and at the source of additional PMOS transistor.

As shown in fig:1 , the w/l ratio or aspect ratio is different for each transistor. For N transistor w/l is taken as 1/1, for P1 transistor it is taken as 2/1 and for P2 transistor w/l value is taken as 5/1.

In this proposed XOR gate V_{dd} is taken as 1V at 0.35µm technology.

On comparing with XOR gates implemented by other technologies it gives less power it gives less power dissipation and delay.

The circuit diagram using Mentor graphics software at 0.35µm technology is shown below with a comparison chart with other XOR gate design.

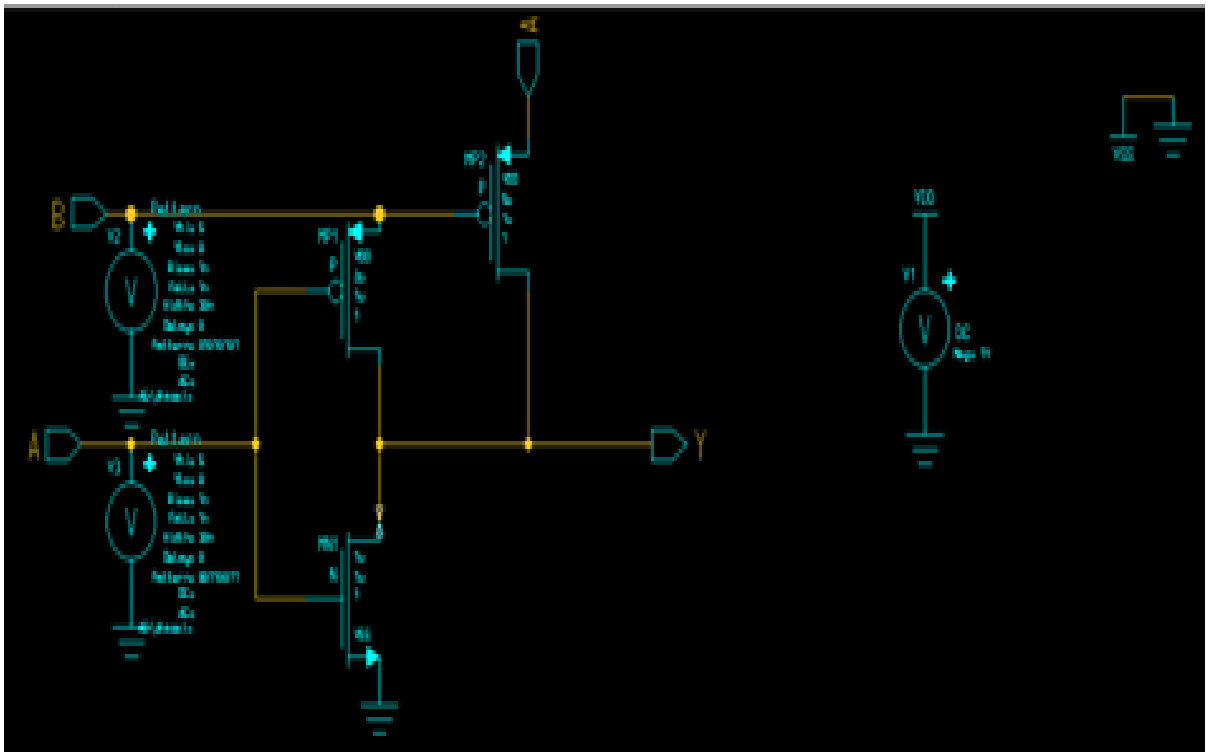


Fig.3: Circuit diagram of 3T XOR gate

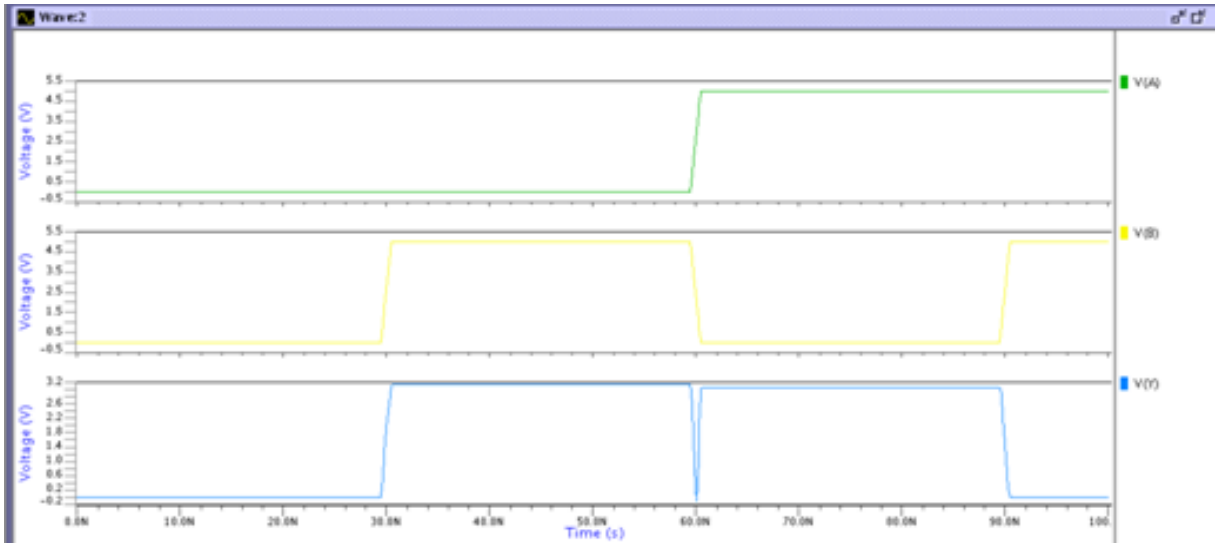


Fig.4: Output Waveform Of 3T XOR

COMPARISION WITH OTHER TECHNIQUES:

S. NO.	CIRCUIT NAME	NO. OF TRANSISTORS	TOTAL POWER DISSIPATION
1.	XOR GATE USING CMOS LOGIC	12T	1.4986n watts
2.	XOR GATE WITH REDUCED TRANSISTOR COUNT	3T	4.0348p watts

3. SIMULATION AND PERFORMANCE ANALYSIS OF THE PROPOSED 3T XOR GATE USING FULL ADDER

Full adders using CMOS logic and using proposed 3T XOR gate are shown below:

In this paper full adder is implemented using proposed 3T XOR gate.

The sum of FA is obtained by connected exclusive OR (EX-OR) gates of the three inputs according to equation 1. The carry of FA is obtained according to equation (2).

FA using CMOS logic consists of 28 transistors which gives more power dissipation.

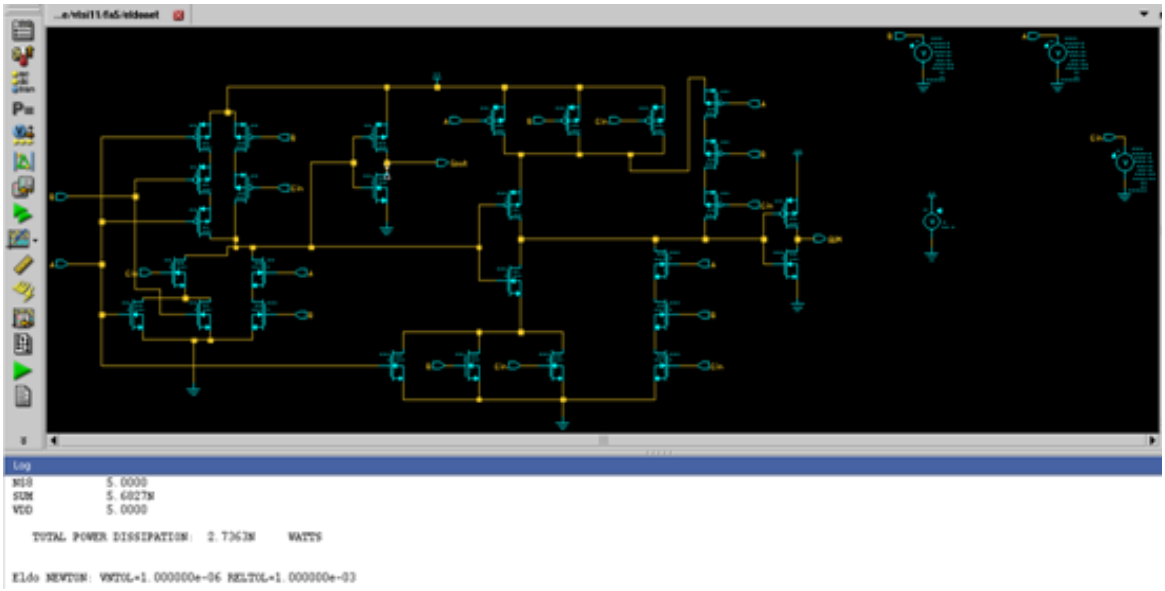


Fig 5: Circuit Diagram Of Full Adder Using CMOS Logic

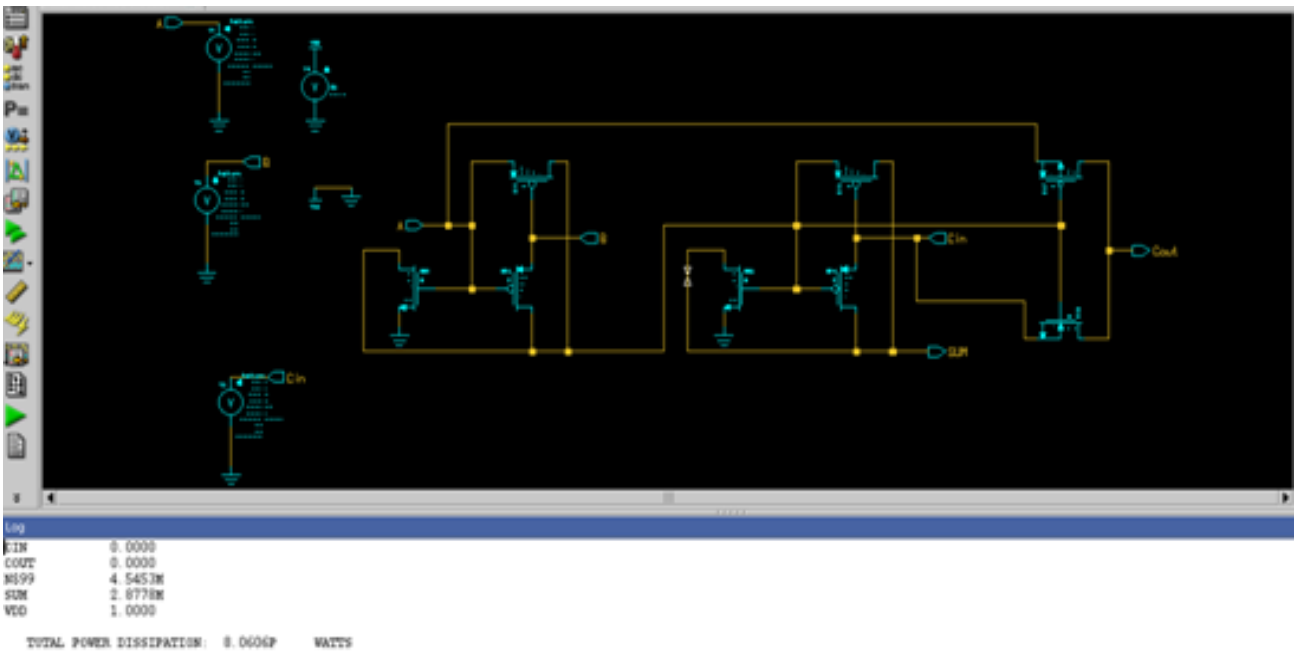


Fig 6: Circuit Diagram Of Full Adder Using 3T XOR gate

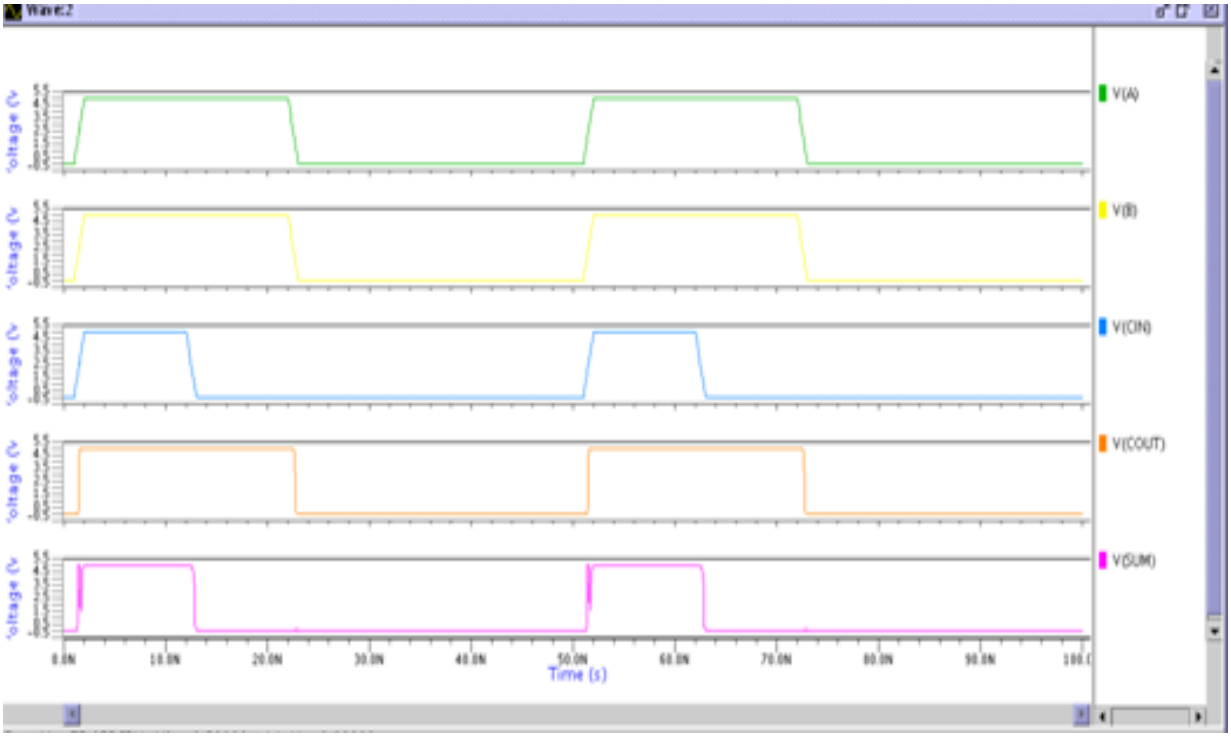


Fig.7: Output Waveform Of Full Adder Using 3T XOR Gate

COMPARISION WITH OTHER TECHNIQUES:

S. NO.	CIRCUIT NAME	NO. OF TRANSISTORS	TOTAL POWER DISSIPATION
1.	FULL ADDER USING CMOS LOGIC	28T	2.7369n watts
2.	FULL ADDER USING PROPOSED 3T XOR GATE	8T	8.0606p watts

4. CONCLUSION

In this paper 16T ripple carry adder is proposed which is based on 8T- full adder. In implementing the ripple carry adder a low power full adder and XOR gate have also been designed. The designed ripple carry adder gives better power dissipation than the other adders mentioned in this paper.

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